REMARKS

Applicants respectfully request reconsideration and allowance in view of the foregoing amendments and following remarks. In the Office Action, mailed January 30, 2004, the Examiner rejected claims 1-18. Following entry of this response, claims 1-18 will be pending in the application.

Specification Informalities

In the Office Action, the Examiner objected to two specification informalities. Specifically, the Examiner noted that on page 18, line 6, the word "retrieve" should be replace with --retrieved--, and that on page 6, line 19, the reference number "18" should actually be --42--. Applicants have, for purposes of readability, corrected these two informalities.

Thus, for at least this reason, Applicants respectfully request withdrawal of these informality objections to the specification.

Drawing Objections

In the Office Action, the Examiner objected to the drawings under 37 C.F.R. §1.84(p)(5) for allegedly including a reference sign "401" that is not mentioned in the description. Applicants respectfully traverse this objection.

The reference sign on which the Examiner is commenting is in the "Key Cache" block of the "Access Point 6" block. Applicants note that the "Key Cache" block, as shown, is reference number "40" and not "401." The line that the Examiner believes to be the numeral "1" of "401" is actually a stray line of the box that surrounds the "Key Cache 40" block. Further, Applicants' specification consistently refers to the "Key Cache" block using reference sign "40" (see, for example, Applicants' Specification, page 6, line 19).

However, notwithstanding the above traversal, Applicants do supply herewith a formal set of all four drawings in the attached Appendix that more definitively illustrate the "Key Cache" block of Figure 1 using reference sign "40."

Therefore, for at least these reasons, Applicants respectfully request entry of these formal drawings and withdrawal of the drawing objections.

Claim Rejections under 35 U.S.C. §103(a)

In the Office Action, the Examiner rejected claims 1-18 under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 5,442,708 to Adams Jr., et al. (hereinafter "Adams") in view of U.S. Patent No. 5,826,109 to Abramson, et al. (hereinafter "Abramson") and further in view of U.S. Patent No. 4,933,938 to Sheehy (hereinafter "Sheehy"). Applicants respectfully traverse the rejections of claims 1-18 and note for subsequent reference the following standards for a proper §103(a) rejection.

A §103(a), or obviousness, rejection is proper only when "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains." 35 U.S.C. §103(a). The Examiner must make out a *prima facie* case for obviousness.

The mere fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness. The *en banc* Federal Circuit has held that "structural similarity between claimed and prior art subject matter, proved by combining references or otherwise, where the prior art gives reason or motivation to make the claimed compositions, creates a prima facie case of obviousness." *In re Dillon*, 16 U.S.P.Q. 2d 1897, 1901 (CAFC 1990).

Further, if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984).

For at least the reasons stated below, Applicants assert that the combination of Adams, Abramson and Sheehy fails to describe or suggest the subject matter as a whole of Applicants' claimed invention and, therefore, that rejected claims 1-18 are patentably distinct from Adams in view of Abramson and Sheehy.

Independent Claims 1, 7 and 13

Applicants' independent claims 1, 7 and 13, generally recite a method of key caching with a system memory and a cache, the system memory and the cache including entries for source addresses and corresponding keys that includes:

receiving a packet from an external source, the packet including a header that is not encrypted and a body that is encrypted;

extracting from the header a source address;

determining whether the source address is included in an entry in the cache;

when the source address is included in an entry of the cache, authorizing an acknowledgment signal for the external source, extracting from the entry of the cache a key corresponding to the source address, and using the key to decrypt the body of the packet;

when the source address is not included in an entry of the cache, determining whether the source address is included in an entry of the system memory; and

when the source address is not included in an entry of the cache and the source address is included in an entry of the system memory, extracting from the entry of the system memory a key corresponding to the source address, and storing the source address and the key as a new entry in the cache.

The Examiner correctly asserts that Adams fails to teach using a cache memory in addition to a system memory as taught by Applicants' independent claims 1, 7 and 13. However, Applicants assert that Abramson and Sheehy do not bridge the gap between the Adams device and Applicants' claimed invention. For at least the following reasons, the cited references neither disclose nor suggest a system as required by independent claims 1, 7 and 13.

Abramson, in general, discloses that "cache memory is a very fast local storage memory that is used by a CPU to hold copies of instructions, code or data that are frequently requested from the main memory by the CPU" (see, Abramson, col. 1, ll. 38-41). However, this teaching does not come close to suggesting the manner in which Applicants' claimed invention uses the key cache. Also, neither Adams nor Sheehy disclose or suggest Applicants' use of the key cache.

Abramson discloses a computer system capable of multiple load operations to the same memory location in the computer system. The Examiner alleges that this is analogous art. It is not, at least not in the context of Applicants' specific use and application of main memory and cache memory in a data communications system. Simply adding cache to the Adams device does not create Applicants' invention, at least not without using a hindsight-focused combination.

For example, the Examiner alleges that Abramson at column 2, lines 1-11 discloses Applicants' invention of "authorizing an acknowledgment signal for the external source." This passage of Abramson states:

> In the prior art, many of these memory subsystems can only accommodate one load operation at a time. This is normally not a problem where there is a hit and the data is forwarded from the cache memory to complete the load operation. However, if there is a cache miss, then a bus cycle must be started to obtain data from an external source. In this case, if another access is made to the cache memory while the other memory operation is pending, the cache memory typically will not accept it, particularly where the access misses the cache. This type of cache is often referred to as a blocking cache. It is desirable to be able to access a cache memory while the cache has other memory operations pending.

As is readily apparent to those skilled in the art, this cited reference has nothing to do with authorizing an acknowledgement to an external source upon determining that the source address, and associated key, is included in the key cache memory. Nobody skilled in the art would combine Abramson to Adams and get anything that even slightly resembled Applicants' invention, at least not without using a hindsight-focused combination.

For at least these reasons, Applicants request the withdrawal and reconsideration of the claim rejections for independent claims 1, 7 and 13. Applicants respectfully submit that independent claims 1, 7 and 13 are in a condition for allowance, and respectfully request a Notice to that effect.

Dependent Claims 2-6, 8-12 and 14-18

Dependent claims 2-6, 8-12 and 14-18 ultimately depend from independent claims 1, 7 and 13, respectively. The allowability of dependent claims 2-6, 8-12 and 14-18 thus follows from the allowability of independent claims 1, 7 and 13, respectively; as such, dependent claims 2-6, 8-12 and 14-18 are allowable over the art of record.

Additionally, with respect to dependent claims 2, 8 and 14, Applicants assert Adams does not disclose or suggest dropping a packet when the source address is not included as an entry in the key cache, as the Examiner alleges. The Adams device is "spliced into the lines of a local area network so that it may intercept all the information flowing into or out of the LAN at the correct layer" (see, Adams, col. 4, ll. 42-45). The Adams device includes a data table stored in main memory that includes a list of sites, destinations, ports and other such routing/handling information, as well as keys for encryption and decryption. The handling instructions of the Adams device dictate when to discard ("toss") data passing through the device (see, Adams, col. 4, ll. 57-67).

Thus, if the ports or destinations do not exist in the network into which the Adams device has been inserted, then all packets to those ports and destination will be discarded ("tossed"). In contrast, Applicants claimed invention of dependent claims 2, 8 and 14 compares the source address to the key cache and, finding no match, drops the packet. This occurs regardless of whether there is a match in the main memory key chain. This sequence means that the external source of the dropped packet, having not received an acknowledgement, will resend the dropped packet. This provides Applicants' invention with time to check the main memory for the necessary key and save it into the cache prior to receiving the resent packet. Adams nowhere discloses such a system.

Additionally, with respect to dependent claims 3, 9 and 15, Applicants assert the cited references do not disclose or suggest sending an acknowledgement to the external source prior to knowing whether the key for data in the received packet exists in the main memory (but after knowing that the key does not exist in the key cache), as the Examiner alleges. The Adams device includes a data table stored in main memory that includes a list of sites, destinations, ports and other such routing/handling information, as well as keys for encryption and decryption. The handling instructions of the Cited references device dictate when to discard ("toss") data passing through the device (see, Cited references, col. 4, ll. 57-67). There is no cache and no decision logic taught or suggested in the cited references that acknowledges receipt of a packet prior to knowing whether the device can even decrypt the received packet. In contrast, Applicants claimed invention of dependent claims 3, 9 and 15 compares the source address to the key cache and, finding no match, authorizes an acknowledgement to the external source. Thus, the external source believes it is free to continue successful transmission. Applicants' device then checks for the proper key for the external device in the main memory, and if it is found, loads the key into the key cache, decrypts the original packet and receives/decrypts any subsequent packets from that external source. The cited references nowhere disclose or suggest such a system.

Therefore, for at least these reasons, Applicants respectfully submit that dependent claims 2-6, 8-12 and 14-18 are in a condition for allowance, and respectfully request a Notice to that effect.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition of allowance and a Notice to that effect is earnestly solicited. If

any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

CHARGE STATEMENT: The Commissioner is hereby authorized to charge fees that may be required relative to this application, or credit any overpayment, to our Account 50-2213, Order No. 073169-0269824 (ATH-026).

Respectfully submitted,
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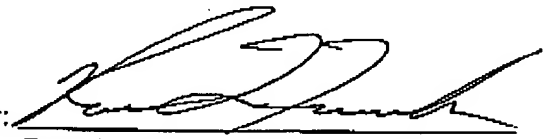
By: 
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